Donald Alpert. Ph.D.
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Donald Alpert, Ph.D., is an independent consultant, specializing in microprocessors and computer systems. For more than a decade in his role as president of Camelback Computer Architecture LLC, Dr. Alpert has provided clients with expert services for patent litigation, technology assessment, and product development. He has over 40 years of wide-ranging academic and industry experience that enable him to provide expert consulting services in the following areas:

- Computers, Computer Systems
- Computer architecture
- Microprocessors
- Semiconductors
- PC Systems
- Embedded Systems
- Design Validation and Debug
- Performance Evaluation
- Cache Memory
- Instruction Sets
- Media Processing
- Power Management

Patent Analysis: Dr. Alpert has served as an expert on dozens of patent litigation cases, handling both infringement and invalidity issues. Dr. Alpert has worked as both a consulting expert and testifying expert assisting attorneys representing major high-tech corporations. He has substantial experience testifying in depositions and at trials before U.S. Federal Courts and the International Trade Commission. Dr. Alpert also consults to assess patents for acquisition and for pre-litigation review. See here for a summary of testifying experience.

Product Development: Dr. Alpert is a widely recognized innovator with over 30 patents. Dr. Alpert has worked at some of the most ground-breaking technology firms, including Zilog, National Semiconductor, and Intel, where he was the principal architect of the Pentium® Processor. See here for more information and example projects.

Employment Experience

Camelback Computer Architecture, LLC, Sacramento, CA
Consultant   2/02-Present
Computer architecture consulting services to assess technology, develop products, and protect IP.

Intel Corporation, Chandler, Arizona
Principal Engineer   12/99-1/02
Led architecture team of 10 responsible for definition and performance evaluation of Itanium™ Processor Family microprocessors.

Principal Engineer   5/98-12/99
Led architecture team of 4 responsible for technical strategy and product definition of PC graphics processors and chipsets.

Stanford University, Stanford, California
Consulting Assistant Professor   9/97-4/98
Responsible for teaching undergraduate and graduate classes in computer architecture and participating in processor-design research projects.

Intel Corporation, Santa Clara, California
Engineering Manager   10/93-6/97
Responsible for microarchitecture definition and architecture validation of the Itanium™ microprocessor, which was the first implementation of Intel's 64-bit extension architecture. Led a team of 60 engineers.

Architecture Manager   1/89-10/93
Responsible for the Pentium® Processor technical definition. Worked with customers and Intel marketing to identify product requirements and with the design engineering team to evaluate design options. Led a team of seven engineers responsible for creating technical specifications and for modeling and simulating performance using traces from DOS, Windows, and UNIX execution. After completing the Pentium Processor, led an interdisciplinary team of 30 engineers to define a new 64-bit instruction set architecture.

National Semiconductor Corporation, Herzlia, Israel
Architecture Manager   5/85-1/89
Responsible for defining new microprocessors in the Series 32000 family, including the NS32532 and "Swordfish" high-performance microprocessors. Led a team of five engineers working in the following areas: modeling and simulating high-performance microprocessors, evaluating novel computer architectures, and writing technical specifications for new products.

Zilog, Incorporated, Campbell, California
Component Architect   6/80-4/85
Worked on the Z80,000 CPU, a 32-bit microprocessor that integrated an instruction pipeline, cache, and memory management unit. Responsible for specifying the non-privileged instruction set, evaluating performance, and writing the reference manual for the microprocessor.

Burroughs Corporation, Pasadena, California
Associate Engineer   7/76-7/77
Designed computer peripheral interface controllers using MSI-TTL and 8080 microprocessors.

Alpex Computer Corporation, Danbury, Connecticut   8/75-6/76
Consulting engineer working on design of video games.

Action, Washington, DC   6/73-6/75
Peace Corps volunteer teaching mathematics and physics in a secondary school in Ghana, West Africa.

Donald Alpert   Camelback Computer Architecture, LLC   (650) 386-5301

Education

Stanford University   9/77-6/84
Graduate study in computer design. National Science Foundation Graduate Fellowship.
Awarded MSEE in 1978 and PhDEE in 1984.

M.I.T.   9/69-6/73
Member of Tau Beta Pi and Eta Kappa Nu. Awarded BSEE in 1973.

Professional Activities

Member of Microprocessor Report editorial board (2002-present)

Anthem College Commencement Address (18-Dec-2009)

Panel session about history of microprocessor development at National Semiconductor Corporation,
Computer History Museum (2008).
[http://archive.computerhistory.org/resources/access/text/Oral_History/102658246.05.01.acc.pdf]

IEEE Technical Committee on Microprocessors and Microcomputers, Chair (1999-2000) and Vice-Chair
(2001-present).

Lectures about the Itanium™ Processor Family at U.C. Irvine (1999, 2000).

Cool Chips I, Keynote speaker (Tokyo, 1998)

IEEE Hot Chips Symposium Program Co-chair (1994), member of program committee (1993, 1995).

Lectures about the Pentium® Processor at Stanford University, University of Illinois, and Cornell (1993-
1994).

Appeared in Stanford UVC Educational Video production about the Pentium Processor (1993).

IEEE International Symposium on Computer Architecture member of program committee (1996) and
Session Chair for Cache Design (1989).

Teaching Experience

Faculty Associate at Arizona State University teaching undergraduate class on assembly language
programming (Spring/2001) and computer architecture (Spring/2002).

Consulting Associate Professor at Stanford University teaching undergraduate and graduate classes in
computer architecture (Fall/1997, Winter/1998).

Consulting Professor at Tel Aviv University teaching graduate class in computer architecture
(Spring/1987)

Peace Corps volunteer in a secondary school in Ghana, West Africa teaching mathematics and physics
(1973-1975).

Publications

Don Alpert, "How Microprocessors Upset the Computer Industry," Microprocessor Report, December 11, 2006.

Don Alpert, "Evolving PC Chip-Set Topologies," Microprocessor Report, April 17, 2006.

Don Alpert, "Will Microprocessors Become Simpler?" Microprocessor Report, November 17, 2003.

Don Alpert, "Itanium Processor Status Report," Microprocessor Report, July 28, 2003.

Don Alpert, "Scalable MicroSupercomputers," Microprocessor Report, March 17, 2003.

Don Alpert, "ColdFire Goes Fully Superscalar," Microprocessor Report, October 28, 2002.

Donald Alpert and Alan Jay Smith, "Guest Editor Introduction," IEEE Micro special issue on Hot Chips VI, April 1995.

Donald Alpert and Dror Avnon, "Architecture of the Pentium Processor," IEEE Micro, June 1993, pp. 11-21. Selected best paper in IEEE Micro for 1993.

D. Alpert, A. Averbuch, and O. Danielli, "Performance Comparison of Load/Store and Symmetric Instruction Set Architectures," Proceedings, 18th International Symposium on Computer Architecture, June 1990, pp. 172-181.

Benjamin Maytal, Sorin Iacobovici, Donald Alpert, et al, "Design Considerations for a General-Purpose Microprocessor," Computer, January 1989, pp. 66-76.

Donald Alpert and Michael Flynn, "Performance Trade-offs for Microprocessor Cache Memories," IEEE Micro, August 1988, pp. 44-54.

D. Alpert, J. Levy, and B. Maytal, "Architecture of the NS32532 Microprocessor," Proceedings, 1987 IEEE International Conference on Computer Design, October 1987, pp. 168-172. Awarded best presenter at Design and Test sessions.

D. Alpert, D. Biran, L. Epstein, et al, "Trends in VLSI Microprocessor Design," Proceedings, First Annual Conference on Computer Technology, Systems and Applications (CompEuro '87), May 1987, pp. 564-567.

Y Sidi, D. Alpert, D. Biran, et al, "Design Considerations of an Advanced 32-Bit Microprocessor," Proceedings, 15th Conference of Electrical and Electronic Engineers in Israel, April 1987.

D. Alpert, "Trends in VLSI Microprocessor Design," Proceedings, 15th Conference of Electrical and Electronic Engineers in Israel, April 1987.

Donald Alpert, Michael J. Flynn, and Scott Wakefield, "Directly Executed Languages for VLSI Processor Design," Proceedings, 1983 IEEE International Conference on Computer Design, October 1983, pp. 609-612.

Donald Alpert, "Powerful 32-Bit Micro Includes Memory Management," Computer Design, October 1983, pp. 213-220.

Don Alpert, Dean Carberry, Mike Yamamura, et al, "32-Bit Processor Chip Integrates Major System Functions," Electronics, July 14, 1983, pp. 113-119.

Patents

4,802,085, Apparatus and method for detecting and handling memory-mapped I/O by a pipelined microprocessor

5,249,286, Selectively locking memory locations within a microprocessor's on-chip cache

5,263,153, Monitoring control flow in a microprocessor

5,416,913, Method and apparatus for dependency checking in a multi-pipelined microprocessor

5,442,756, Branch prediction and resolution apparatus for a superscalar computer processor

5,475,824, Microprocessor with apparatus for parallel execution of instructions

5,479,652, Microprocessor with an external command mode for diagnosis and debugging

5,481,751, Apparatus and method for storing partially-decoded instructions in the instruction cache of a CPU having multiple execution units

5,559,986, Interleaved cache for multiple accesses per clock cycle in a microprocessor

5,606,676, Branch prediction and resolution apparatus for a superscalar computer processor

5,617,554, Physical address size selection and page size selection in an address translator

5,621,886, Method and apparatus for providing efficient software debugging

5,638,525, Processor capable of executing programs that contain RISC and CISC instructions

5,657,253, Apparatus for monitoring the performance of a microprocessor

5,659,679, Method and apparatus for providing breakpoints on taken jumps and for providing software profiling in a computer system

5,669,011, Partially decoded instruction cache

5,671,435, Technique for software to identify features implemented in a processor

5,675,825, Apparatus and method for identifying a computer microprocessor

5,692,167, Method for verifying the correct processing of pipelined instructions including branch instructions and self-modifying code in a microprocessor

5,729,724, Adaptive 128-bit floating point load and store operations for quadruple precision compatibility

5,740,413, Method and apparatus for providing address breakpoints, branch breakpoints, and single stepping

5,764,959, Adaptive 128-bit floating point load and store instructions for quad-precision compatibility

5,774,686, Method and apparatus for providing two system architectures in a processor

5,790,834, Apparatus and method using an ID instruction to identify a computer microprocessor

5,802,605, Physical address selection and page size selection in an address translator

5,958,037, Apparatus and method for identifying features and the origin of a computer microprocessor

5,991,874, Conditional move using a compare instruction generating a condition field

6,052,801, Method and apparatus for providing breakpoints on a selectable address range

6,219,774, Address translation with/bypassing intermediate segmentation translation to accommodate two different instruction set architecture

6,385,718, Computer system and method for executing interrupt instructions in operating modes

6,408,386, Method and apparatus for providing event handling functionality in a computer system

6,584,558, Article for providing event handling functionality in a processor supporting different instruction sets

7,010,671, Computer system and method for executing interrupt instructions in two operating modes

7,389,403, Adaptive computing ensemble microprocessor architecture

7,802,073, Virtual core management